Hydrogen Test on EFA072A and EFA025A

Background

It was reported from the field that when EFA072A devices from W234-2 were life tested in hydrogen environment, the Idss of the DUT has increased by 15% or so in a few days. However, when the devices were life tested in open air environment, no Idss increase was observed.
To investigate this phenomenon, we have repeated the test and also compared the result with those from the other wafers in the same conditions.

Introduction

Ever since the hydrogen effect or so-called hydrogen poisoning effect was first reported in 1989 by the IBM group, numerous papers about this effect were published. So far, workers have found that the Idss of GaAs MESFET and PHEMT invariably decrease in this condition. The Idss of InP PHEMT, however, was reported to increase in the same condition.
The mechanism of this phenomenon is still not well concurred among the workers, but it has been accepted that Pt or Pd used in gate structure in many manufactures are converting atomic hydrogen into molecular one by catalytic reaction, and the converted molecular hydrogen is now able to defuse into the channel under or near gate to compensate the donors and thus to cause the hydrogen poisoning effect.
Since hydrogen can be desorbed from plated Au, Kovar, and microwave absorber inside a hermetically sealed package, this hydrogen poisoning effect was first observed in this environment and has become one of the prime reliability concerns.

Discussion

In order to circumvent this effect, many approaches have been adopted and many of which were shown to be very effective.

1. Majority of US manufactures has developed Ti-Pt-Au gate by historical reason, and their production has been based on this structure. Rather than changing the gate structure to disturb the production flow, most of them has opted to use hydrogen getter to reduce the effect.
2. There are many other gate structures fabricated without using Pt or Pd and they are shown to be immune to this effect. The reported gate materials are Al, Mo, Ti-W, W, and W-Si, most of which were developed by non-US manufactures. Notable, in US, Ti-W/Au gate has been developed by Avantek and TiN-WSi/Au or TiN-TiW/Au by MwT, and they are also completely immune to H2.
3. The gate structure used by the above two manufactures, in which Ti or TiN layer wraps entirely under side of Y shaped gate, is also found to be effective in eliminating the hydrogen effect in Ti-Pt-Au structure by Litton and Excelics. Ti is acting as a diffusion barrier to Pt and there is no exposed Pt near vicinity of GaAs.
   In Excelics' structure, 800 angstrom of Ti is completely wrapping the underside of Y or V shaped gate. This structure has been found to be completely immune to the hydrogen effect and no detrimental effect by H2 is observed.

The report of the Idss increase in EFA072A due to hydrogen was, hence, out of ordinary. We expect no hydrogen poisoning effect to Excelics' devices and if do, we expect Idss to decrease.

Hydrogen Test

To reproduce the reported anomaly, we have assembled devices from EFA072A/W234-2 and W234-3 in open carrier, mounted in an enclosed jig, and bias stressed (Vds=8.0V, Ids=0.5Idss) at base temperature of 100ºC in forming gas (5% H2, 95% N2). The hydrogen test set-up and overview are shown in figure 1.
Also to compare and repeat our existing test result, devices from EPA025/W365-2 and EFA025/W394-4 were assembled and hydrogen tested side by side with the EFA072A.

Test Result

As reported in a separate memo, EPA025/W365-2 (PHEMT) and EFA025/W394-4 (MESFET) did not show any sign of hydrogen poisoning effect.
However, EFA072A has indeed reproduced the Idss increase as has been reported. Results obtained from W334-2 are illustrated in figure 2. Vp and Igq (Igs at Vds=8V, Ids=0.5xIdss) showed similar increase in magnitude as illustrated in figure 5.
We have also observed that the Idss does not increase when the same device is stressed in the air environment, figure 3. When the devices were stressed sequentially in air and H2 or in reverse sequence, Idss has increased in respect to H2 environment, figure 4. The RF performance, particularly gain and power output did not show any significant changes

for the both burn-in cases. We have also measured IMD3, and the results appear to indicate that H2 stress may be causing IMD3 to improve. We need more data points to come to a tentative conclusion.
Very similar results were obtained from the other wafer which was fabricated in the same lot (W234-3). Idss and Gm as a function of stress in H2 and air are illustrated in figure 6.

Analysis
It was recalled by our technical officer that the EFA072/W234 along with a few other wafer lots were fabricated using non-standard Si3N4 passivation layer. Because of our Si3N4 equipment problem, we had used an optical device house to have Si3N4 deposited onto these wafer lots. We deduced that the stress of that layer was marginal for the surface device like ours. The electron traps generated by the built-in stress must have been restricting the electron flow in the channel. H2 environment and localized heating from DC bias at elevated base temperature appear to anneal out the damage at the Si3N4 to GaAs interface.
To test whether or not hydrogen, elevated temperature, and transistor current are equally contributing to this effect, we have baked the suspect devices in H2 or in air without DC bias applied to the devices. We have also bake-tested EFA025A/W232-4, which had the same Si3N4 coated at the same time. The results obtained from 10 devices from EFA072A and 5 devices from EFA025A are tabulated, as well as the initial bias stressed data.

All three wafers tested above show very similar behavior like the first test with DC bias, namely, Idss has increased by 10.5 to 12.8% for the H2 bake and only -0.8 to 1.1% for the air bake as tabulated in Table 1, 2, & 3.
Another observation is that gate breakdown voltage, after stressed in H2 or air, has degraded appreciably for EFA072A, whereas those of EFA025A has little change. This may be due to a process variation at Si3N4 step.

Wafer EFA072A	Stress condition	ΔIdss (%)	ΔGm (%)	ΔVp (V)
W234-2	H2	12.8%	-13.2%	-0.46
	Air	-1.0%	2.3%	-0.02
W234-3	H2	14.1%	-12.3%	-0.60
	Air	-2.8%	1.4%	-0.05

Table 1. Deltas for Bias Stressed at 100ºC in H2 or Air

Wafer EFA072A	Bake condition	ΔIdss (%)	ΔGm (%)	ΔVp (V)	ΔBVgd (V)	ΔBVgs (V)
W234-2	H2	12.8%	-7.17%	-0.50	2.5	2.7
	Air	0.4%	3.8%	-0.19	2.2	2.2
W234-3	H2	12.3%	-12.0%	-0.51	2.8	2.3
	Air	1.1%	5.2%	-0.19	2.5	2.2

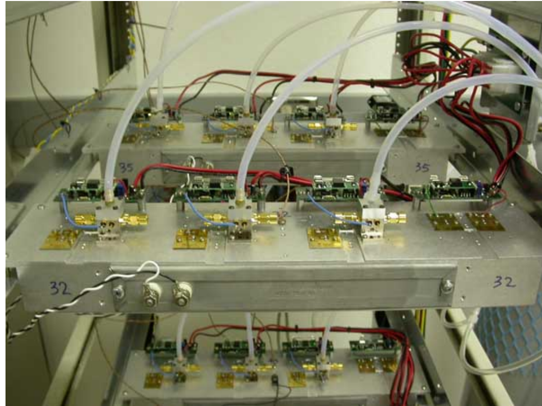
Table 2. Deltas for H2 or Air Baked at 150ºC for EFA072A

Wafer EFA025A	Bake condition	ΔIdss (%)	ΔGm (%)	ΔVp (V)	ΔBVgd (V)	ΔBVgs (V)
W232-4	H2	10.5%	-5.6%	-0.28	0.5	0
	Air	-0.8%	-2.2%	0.05	0.25	-0.25

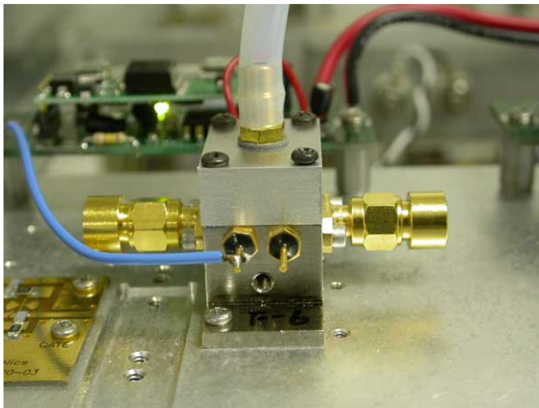
Table 3. Deltas for H2 or Air Baked at 150ºC for EFA025A

Conclusion
We can thus conclude that hydrogen is the major factor to this phenomenon; the air alone without hydrogen does not introduce the annealing effect, and DC bias has little effect.
We can also conclude that this anomaly is unique and isolated case where non-standard Si3N4 was used for passivation layer. All three wafers tested have exhibited almost unchanged RF characteristic after the Idss had increased. Some wafers, however, are possibly reliability hazard due to BVg degradation, while the other wafer (EFA025A/W232-4) did not exhibit the same trend.
The corrective action is not to use non-approved Si3N4 layer for passivation in the future and purge the wafers which exhibit rapid gate breakdown voltage degradation in H2 and Air (EFA072/W234-2 and -3). The wafers which do not exhibit the BVg degradation can be used as is.

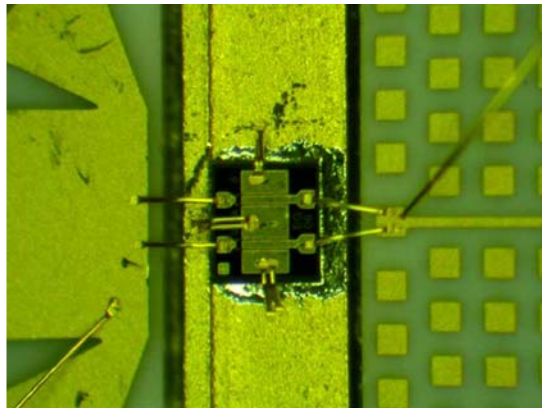
Burn-in Setup Overview



Burn-in Jig Overview



Burn-in Jig Close up View



EFA072 in Burn-in and Test Circuit

Figure 1 Burn-in of EFA072 in Hydrogen Environment

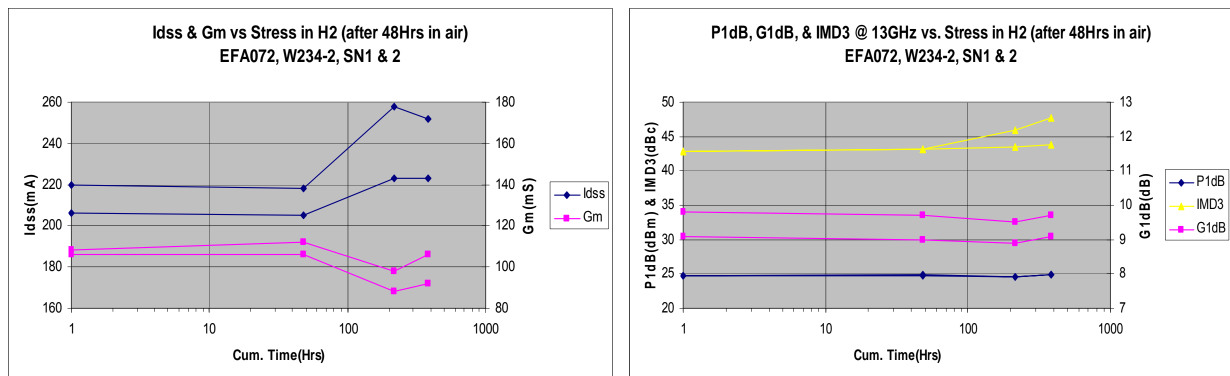
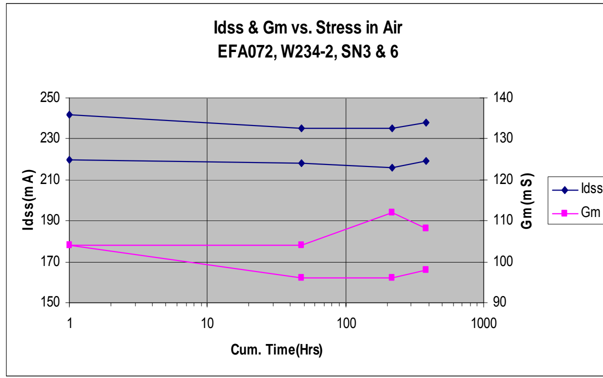


Figure 2. Result of Burn-in for 336Hrs in H2 after 48Hrs in Air



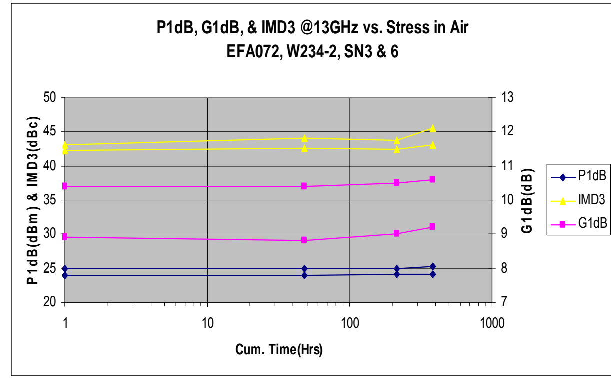
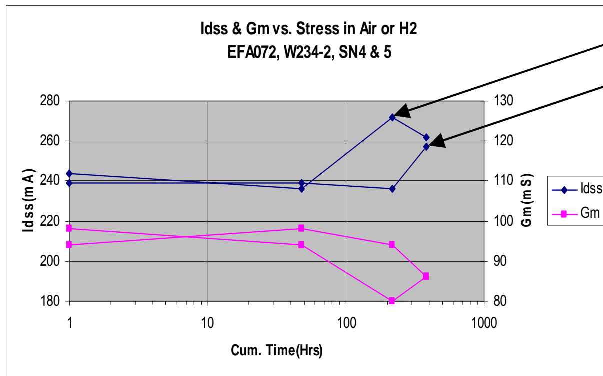


Figure 3. Result of Burn-in for 384Hrs in Air



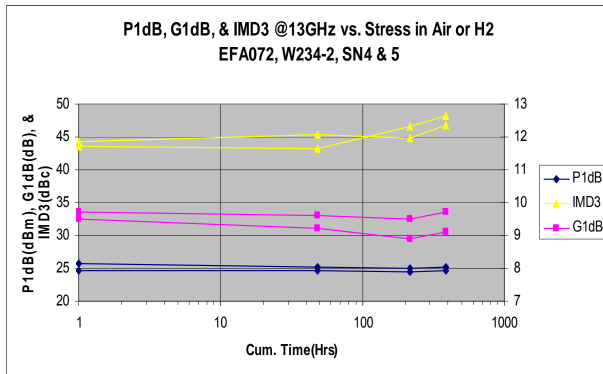


Figure 4. Result of Burn-in in Air and H2

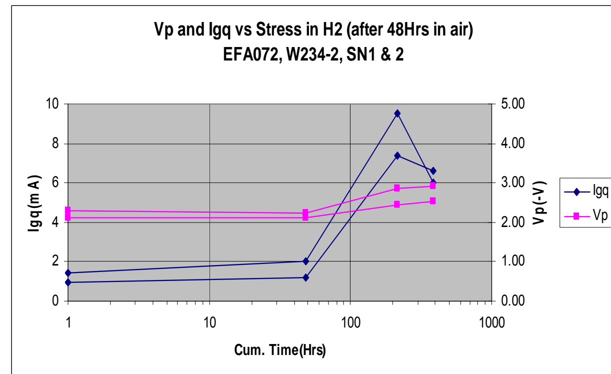


Figure 5. Vp & Igq Change due to H2 Stress

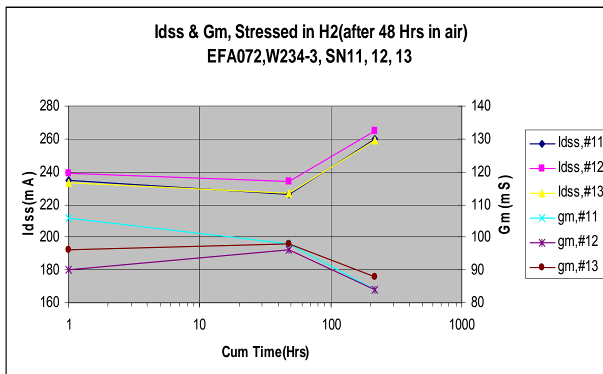


Figure 6a. Result of B-in in Air (48hrs) + H2 (168hrs)

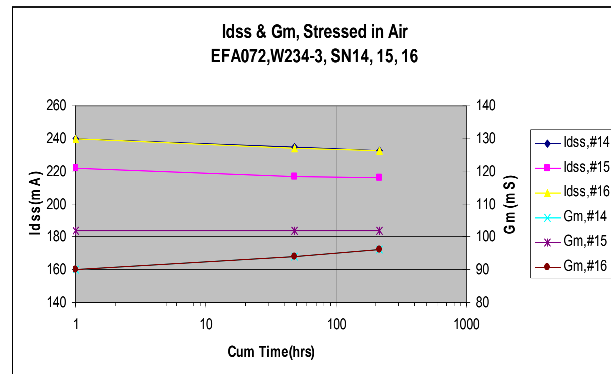


Figure 6b. Result of B-in in Air only