

Recommendations for the Handling, Mounting and Biasing of High Power GaAs FETs

A. Handling Precautions:

All GaAs FETs are sensitive to electrostatic discharge. It is Excelics policy that all GaAs FETs will be shipped in electrostatic protective packaging and the user must pay careful attention to the following precautions when handling FETs:

- 1) Personnel handling GaAs FETs should ensure that they are properly grounded by a wrist strap or equivalent.
- 2) When mounting the FET in a circuit, the circuit gate and drain connections should be shorted to ground.
- 3) When soldering the FET leads, it is recommended that an ESD approved iron be utilized.

B. Device Mounting Instructions:

For best performance and high reliability a good thermal interface between the GaAs FET package flange and the heat sink is essential.

- 1) Heat Sink: The amplifier case or heat sink should be made of copper or aluminum and its surface nickel or tin plated.

Caution: Silicon based heat sink compound should not be used. These products contribute to poor grounding of the source flange while having the potential to introduce contamination and possible long term degradation of thermal resistance between the FET package and the heat sink.

- 2) Mounting Surface:

Surface Finish: 50µm maximum

Camber: ± 10 µm maximum

Note: Be certain that the mounting surface is free of any debris before attaching the device. Trapped particles between the device and the heat sink will drastically reduce the transfer of heat from the device to the heat sink thus reducing the MTTF and reducing the device performance.

- 3) Screw Mounting: The flange may be attached using screws. The recommended torque values, by package type, are listed below.

Package	Recommended Torque	Maximum Torque
180F	2.5 Kg-cm (2.2 lb-in)	3.0 Kg-cm (2.6 lb-in)
382	4.5 Kg-cm (3.9 lb-in)	5.0 Kg-cm (4.3 lb-in)
508	4.5 Kg-cm (3.9 lb-in)	5.0 Kg-cm (4.3 lb-in)

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C. Bias Circuit

This application note is intended to instruct the user in proper DC biasing of Excelics high power GaAs FETs.

- 1) DC Supply: When applying DC bias to a device in a common source configuration, a negative gate voltage must be applied first, followed by a positive drain voltage. Conversely, when removing the DC bias, the drain voltage must be removed first followed by the gate voltage. A GaAs FET with drain voltage applied, and floating or zero gate voltage, is likely to oscillate and may damage the FET.

Reference Fig. 2

- 2) Bias Application Circuit: A self-sequencing, fault-protected bias supply is recommended.

Recommended Source: Teedia, Inc.

- 3) RF Bias Circuit: The injection of bias voltages into a GaAs FET RF circuit is typically accomplished via quarter wavelength transmission lines. This configuration, as shown in Fig. 3, is intended to provide the DC connection to the GaAs FET gate and drain, with minimal impact to the device RF performance.

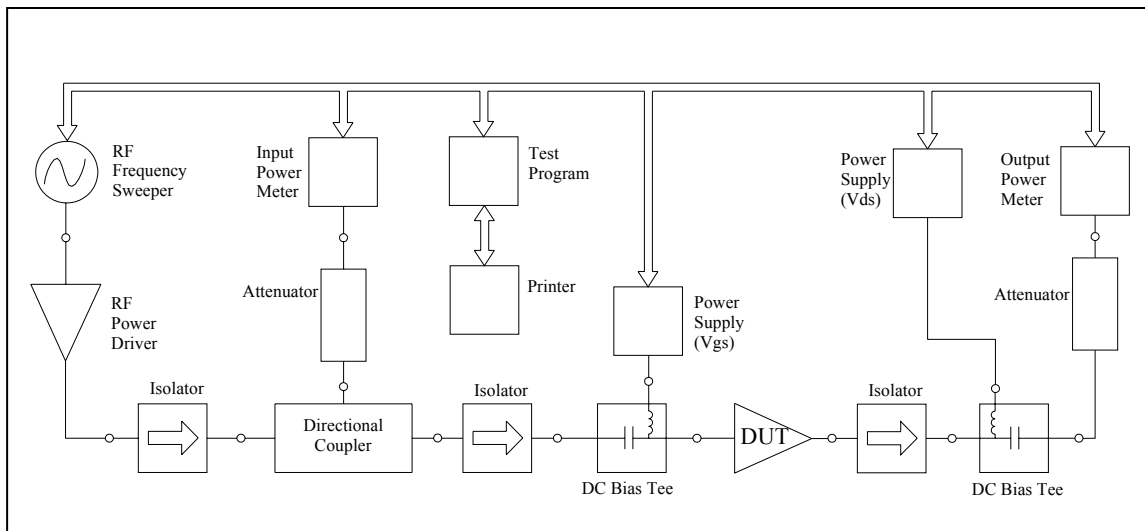


Figure 1: Power Test Set-Up Block Diagram

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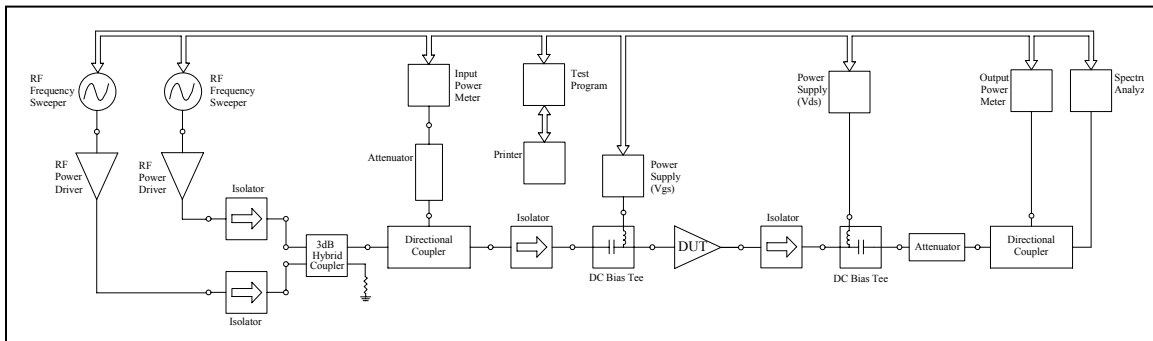


Figure 2: IM3 Test Set-Up Block Diagram

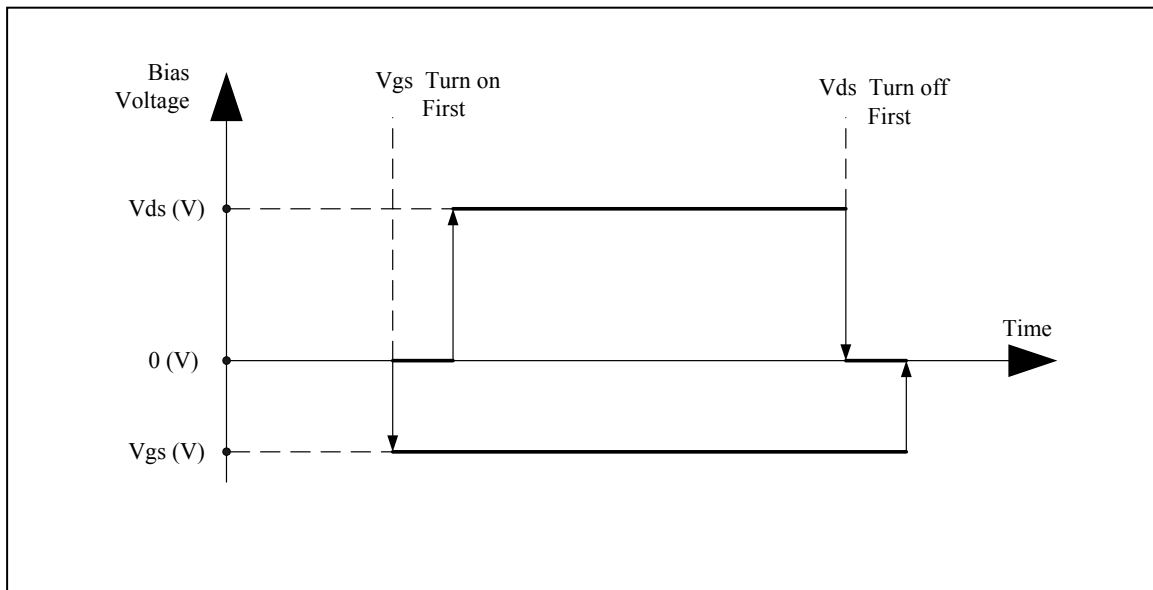


Figure 3: DC Bias Sequence

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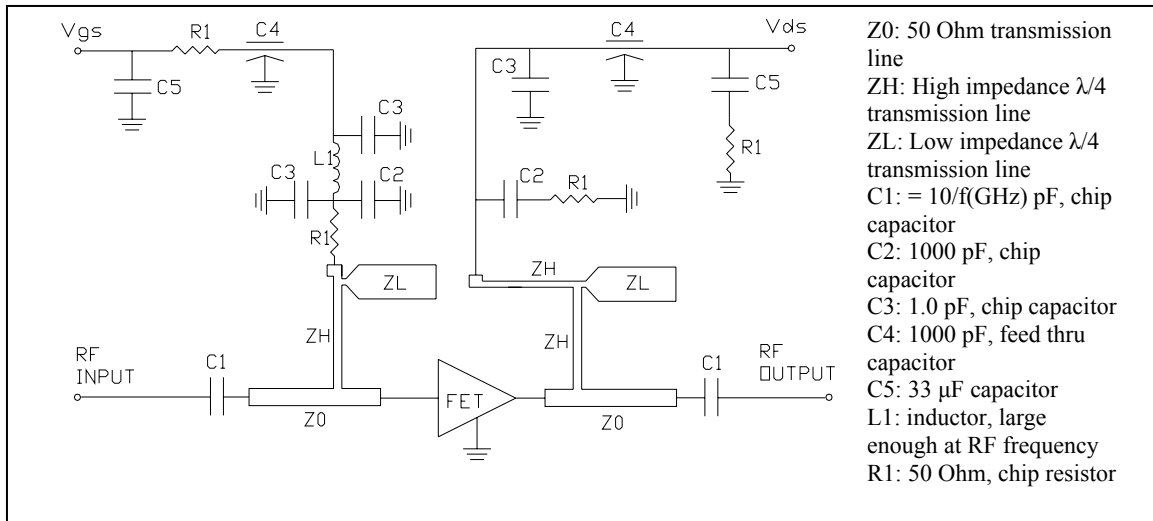


Figure 4: Reference RF and Decoupling Circuit for Internally Matched FETs

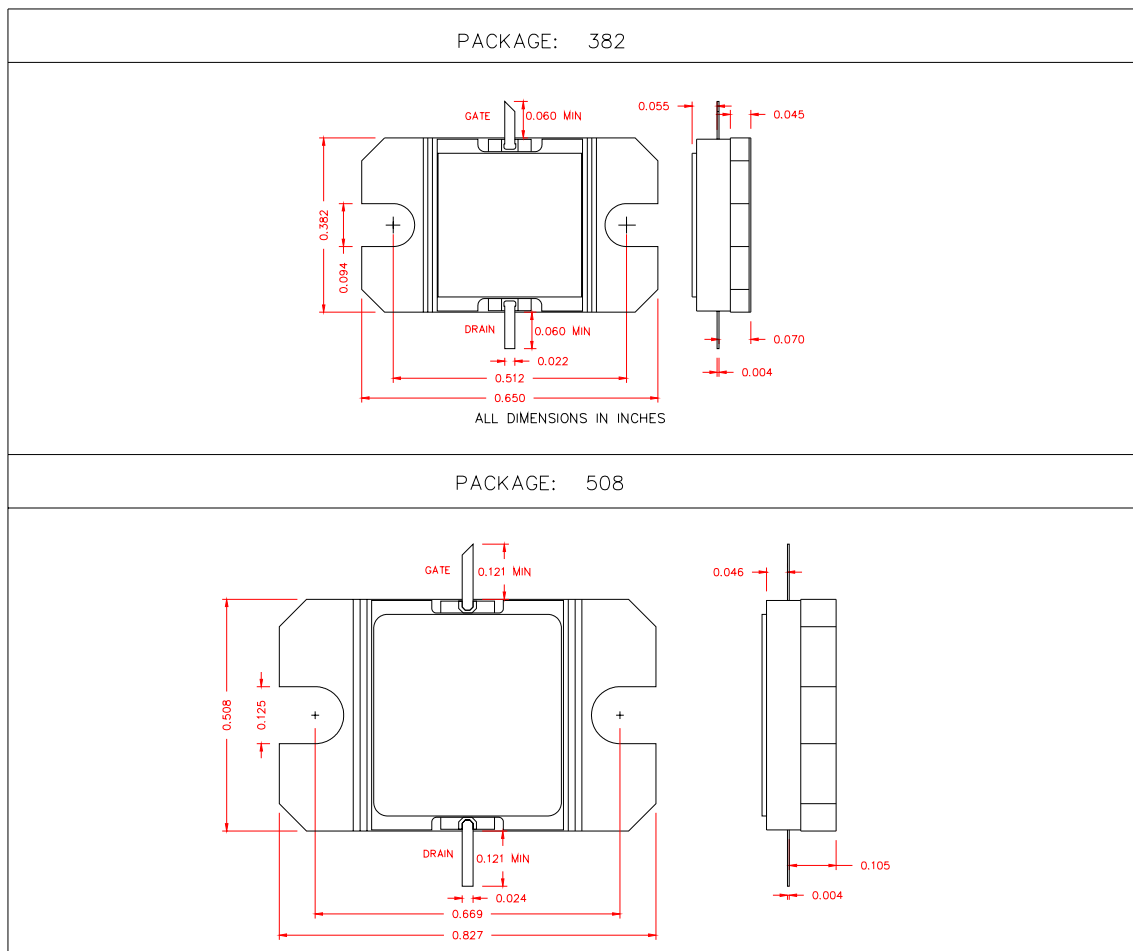


Figure 5: Package Outlines