

RELIABILITY TESTS for EXCELICS' FETs

A.) HIGH TEMPERATURE D.C. BIAS BURN-IN AND MTTF PREDICTION:

1.) GaAs Power FET (EFA060B): (Total 24 devices from 3 wafers)

D.C. Biased at 8V and 50% Idss, Burn in at $T_{\text{junction}} = 225$ and 205°C .

Failure Criteria: All data sheet D.C. parameters (Idss, Gm, Vp, Vbgs, Vbgd) variations > -20% pre- and post burn-in.

$T_{\text{junction}} = 205^{\circ}\text{C}$: Burned in 1,000 hours showing all D.C. parameter variations < -10%, 0/12 failure.

$T_{\text{junction}} = 225^{\circ}\text{C}$: Burned in 1,000 hours showing 5/12 failure, Projected MTTF = 3,300 hours.

Long term failure mechanism : : a gradual decrease in saturated current and transconduction, resulting from ohmic degradation.
 no degradation in gate metal quality.
 Projected Failure Activation Energy = 1.6 eV

$T_{\text{junction}} (^{\circ}\text{C})$	200	175	150	125	100	75	50	25
MTTF (hours)	2.4×10^4	2.2×10^5	2.4×10^6	4.0×10^7	9.0×10^8	3.1×10^{10}	2.0×10^{12}	2.4×10^{14}

2.) Heterojunction Power FET (EPA025A): (Total 24 devices from 3 wafers)

D.C. Biased at 8V and 50% Idss, Burn in at $T_{\text{junction}} = 210$ and 190°C .

Failure Criteria: All data sheet D.C. parameters (Idss, Gm, Vp, Vbgs, Vbgd) variations > -20% pre- and post burn-in.

$T_{\text{junction}} = 190^{\circ}\text{C}$: Burned in 18,363 hours showing 1/12 failure.

$T_{\text{junction}} = 210^{\circ}\text{C}$: Burned in 18,363 hours showing 3/12 failure.

Projected MTTF = 2.2×10^5 hours at $T_{\text{junction}} = 210^{\circ}\text{C}$ and MTTF = 2.0×10^6 hours at $T_{\text{junction}} = 190^{\circ}\text{C}$

Yielded projected Failure Activation Energy = 2.1 eV

$T_{\text{junction}} (^{\circ}\text{C})$	200	175	150	125	100	75	50	25
MTTF (hours)	6.6×10^5	1.2×10^7	4.1×10^8	9.7×10^9	6.0×10^{11}	6.7×10^{13}	1.2×10^{16}	6.9×10^{18}

B.) R.F. HIGH POWER DRIVE TESTS:

$P_{\text{OUT}} = P_{-6} (\sim P_{\text{SAT}})$ CW for >15 hours at room temperature with D.C. biased at

8V and 50% Idss for GaAs power FETs and 8V and 50% Idss for Heterojunction power FETs:

Failure Criteria: All data sheet D.C. parameter (Idss, Gm, Vp, Vbgs, Vbgd) variations > +10%,
 R.F. parameter ($P_{-1/-6\text{dB}}$ & $G_{-1/-6\text{dB}}$) variations > +0.75 dB or dBm,
 pre- and post high power drive.

No significant changes observed in D.C. & R.F. parameters post high power drive tests for GaAs and heterojunction power FETs.

C.) 300°C STORAGE BAKE:

For EFA060B devices, all DC parameters changed less than 5% after 40 Hrs. bake with total of 12 devices from 4 wafers.

For EPA025A devices, all DC parameters changed less than 10% after 94 Hrs. bake with total of 28 devices from 3 wafers.